REMARKS

Applicants hereby amend the specification and claims 4, 10-12, 27, 34-35, and 37-38.

In view of the foregoing, an early action on the merits is hereby solicited.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

Respectfully submitted,

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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The specification is changed as follows:

Page 1, paragraph starting in line 29 is amended as follows:

However, a satisfactory oxide film that satisfies the requirements with regard to interface characteristics of the oxide/Si substrate interface, breakdown characteristics, and leakage current characteristics, is obtained only when the surface of the Si substrate has a (100) orientation as far as thermal oxidation process is used. When a thermal oxidation process is applied to a Si substrate having a surface orientation other than the (100) surface for forming a gate oxide film, there arises various problems in the gate oxide film such as increased surface state density at the oxide/Si substrate interface as compared with case of forming the Si oxide film on the (100)-oriented Si substrate. Further, the oxide film thus formed suffers from the problem of poor breakdown voltage characteristics or poor leakage current characteristics.

Page 7, paragraph starting in line 11 is amended as follows:

According to the present invention, active hydrogen nitride radicals NH* are formed efficiently by activating NH_3 or a mixed gas of N_2 and H_2 in microwave exited plasma of Ar or Kr. By causing the hydrogen nitride radicals NH_3* to react, it becomes possible to form a silicon nitride film having a quality superior to a silicon thermal oxide film formed at about 1000°C on the (111) surface of a Si crystal at a low temperature of 550°C or less. The silicon nitride film thus formed can be used as a high-dielectric gate insulation film and it becomes possible to form a high-performance semiconductor device or a high-performance semiconductor integrated circuit device on the (111) surface of the Si crystal. It should be noted that the (111) surface of the Si crystal may be the one defining the principal surface of a Si single crystal substrate or the one formed in a part thereof. Further, the (111) surface may be the one appearing at the surface of a polysilicon film.

Page 12, paragraph starting in line 28 is amended as follows:

FIG. 2 shows the thickness of the oxide film for the case in which the total pressure inside the processing chamber 101 is changed while maintaining the Kr and oxygen pressure ration such that the proportion of Kr is 97% and the proportion of oxygen is 3%. In the experiment of FIG. [3]2, it should be noted that the silicon substrate was held at 400°C and the oxidation was conducted over the duration of 10 minutes.

Page 28, the paragraph starting in line 2 is amended as follows:

FIGS. 10[(]A[)] – 10[(]D[)] show the fabrication process of a MIS transistor according to a first embodiment of the present invention.

Page 28, the paragraph starting in line 5 is amended as follows:

Referring to FIG. 10[(]A[)], a stacked gate insulation film 12 is formed on a (100) principal surface or a (111) principal surface of a Si substrate 11, by depositing a Si oxide film 12A and a Si nitride film 12B with respective thicknesses of 1 nm and 2 nm by conducting the process steps explained before in the substrate processing apparatus of FIG. 1. Next, in the step of FIG. 10[(]B[)], a polysilicon film 13 is deposited on the stacked gate insulation film 12.

Page 28, the paragraph starting in line 14 is amended as follows:

Next, in the step of FIG. [(]C[)], the polysilicon film 13 is patterned into a gate electrode 13A, and ion implantation process of impurity element is conducted into the Si substrate 11 while using the gate electrode 13A as a mask. As a result, LDD regions 11A and 11B are formed in the substrate 11 at both lateral sides of the gate electrode 13A.

Page 28, the paragraph starting in line 22 is amended as follows:

Next, in the step of FIG. 10[(]D[)], sidewall insulation films 14A and 14B are formed on respective sidewall surfaces of the gate electrode 13A, and high-concentration diffusion regions 11C and 11D are formed in the substrate 11 at outer regions of the sidewall insulation films 14A and 14B as source and drain regions of the MIS transistor. The diffusion regions

11C and 11D are formed by conducting an ion implantation process of an impurity element while using the sidewall insulation films 14A and 14B as a mask.

Page 29, the paragraph starting in line 8 is amended as follows:

Measurement of the channel mobility conducted on the MIS transistor of FIG. 10[(]D[)] with regard to the surface orientation dependence of the channel mobility has revealed the fact that the channel mobility increases by the factor of about 1.2 or more in the transistor formed on the (111)-oriented Si substrate as compared with the transistor formed on the (100)-oriented Si substrate, irrespective of whether the MIS transistor is an n-channel transistor or the MIS transistor is a p-channel transistor.

Page 34, the paragraph starting in line 1 is amended as follows:

Typically, the ferroelectric film 1106 is formed by a sputtering process such that there appears a Sr: Ta: Nb of 1:0.7:0.3 in the ferroelectric film, and a plasma oxidation process is conducted thereafter at the temperature of 400°C by carrying out the Kr/O_2 plasma oxidation processing explained before. As a result, the ferroelectric film 1106 has a composition represented as [Sr2(Ta0.7Nb0.3)2O7] $\underline{Sr_2(Ta_{0.7}Nb_{0.3})_2O_7}$.

Page 35, the paragraph starting in line 23 is amended as follows:

In conventional ferroelectric memory devices, the ferroelectric film 1106 of the SrTaNbO system has been formed by a sol-gel process, followed by a crystallization process conducted by a thermal annealing process at high temperature of 900°C or more. However, the ferroelectric film formed by such a conventional process has suffered from the problem of inhomogeneous film composition and deterioration of device performance that is caused by elemental diffusion associated with the use of high temperature. Further, the ferroelectric film thus formed shows a poor leakage characteristic. On the contrary, the present invention enables formation of a high-quality [Sr2(Ta0.7Nb0.3)2O7] $\underline{Sr_2(Ta_{0.7}Nb_{0.3})_2O_7}$ film characterized by the features of excellent uniformity, free from element diffusion, excellent leakage current characteristic, and the like, by accurately controlling the Sr: Ta: Nb ratio to 1:0.7:0.3 in the sputtering process of the [StTaNbO] $\underline{SrTaNbO}$ film and further by applying the Kr/O_2 plasma oxidation process at low temperature.

Page 44, the paragraph starting in line 32 is amended as follows:

The channel layers 1503 and 1504 are covered by an insulation film 1509, and a polysilicon gate electrode 1510 is formed on the channel layer 1503 via the insulation film 1509. Similarly, a polysilicon gate electrode 1511 is formed on the channel layer 1504 via the insulation film 1509. Further, an insulation film 1512 of SiO_2, BSG or BPSG is formed on the Si_3N_4 film 1502 so as to cover the channel layers 1503 and 1504 and further the gate electrodes 1510 and 1511, and a source electrode 1513 and a drain electrode 1514 are formed on the insulation film 1512 respectively in contact with the source region 1505 and the region 1506. It should be noted that the drain electrode 1514 function also as the source [region] electrode of the p-MOS transistor formed on the channel layer 1504 and thus makes a contact with the source region 1507 via the insulation film 1512. Further, a source electrode 1515 of the p-MOS TFT is formed on the insulation film 1512, wherein the source electrode 1515 makes a contact with the drain region 1508 via the insulation film.

Page 49, the paragraph starting in line 14 is amended as follows:

It should be noted that the foregoing description is not limited to the (111) surface of the Si crystal but is valid also with a crystal surface near the (111) surface with an offset angle [of less than ± (*** to be added ***)] in an arbitrary direction from the (111) surface.

IN THE CLAIMS:

The claims are amended as follows:

4. (Amended) A semiconductor device as claimed in claim 1, [characterized in that] wherein said Si oxide film contains Kr with a surface density of $5 \times 10^{11} cm^{-2}$ or less at a surface thereof.

10. (Amended) A semiconductor device as claimed in claim 9, [characterized in that] wherein said Si nitride film contains Ar or Kr with a surface density of $5 \times 10^{11} cm^{-2}$ or less.

11. (Amended) A semiconductor device as claimed in claim 9, [characterized in that] wherein said Si nitride film contains hydrogen atoms therein.

12. (Amended) A semiconductor device as claimed in claim [6] 9, [characterized by] further comprising a gate electrode on said Si nitride film.

27. (Amended) A ferroelectric memory device, [characterized by] comprising:

a Si substrate;

a gate insulation film formed on said Si substrate;

a gate electrode of polysilicon formed on said gate insulation film;

a Si nitride film formed on said gate insulation film; and

a ferroelectric film formed on said Si nitride film; and

another electrode formed on said ferroelectric film, said Si nitride film containing Ar or Kr.

34. (Amended) A method of forming a Si nitride film as claimed in claim 33, wherein said [oxidation] nitriding step is conducted at a temperature of 550°C or less.

35. (Amended) A method of forming a Si nitride film as claimed in claim 33, wherein said [oxidation] nitriding step is conducted at a temperature of about 400°C.

37. (Amended) A method of forming an oxide film on a polysilicon pattern, characterized by the steps of:

forming a polysilicon pattern on an insulation film; and

oxidizing a surface and a sidewall of said polysilcion [film] pattern to form an oxide film such that said oxide film covers said surface and said sidewall of said polysilicon [film] pattern continuously,

said step of forming said oxide film comprising the steps of:

forming plasma by exciting an inert gas predominantly of Kr and an oxygen gas by a microwave; and

oxidizing a surface of said polysilicon [film] pattern by atomic state oxygen O* formed with excitation of said plasma.

38. (Amended) A method of forming a nitride film on a polysilicon pattern, characterized by the steps of:

forming a polysilicon pattern on an insulation film; and

forming a nitride film by nitriding a surface and sidewall of said polysilicon [film] pattern such that said nitride film covers said surface and said sidewall of said polysilicon [film] pattern continuously;

said step of forming said nitride film comprising the steps of:

forming plasma by exciting an inert gas predominantly of Ar or Kr and a gas containing nitrogen as a constituent element by a microwave; and

nitriding a surface of said polysilicon [film] pattern by hydrogen nitride radicals NH* formed with excitation of said plasma.